Ref. Des.	Marking	Description	Function	Location (See Note.)
J1		Conn, 2x22 card edge	Rear Detector Conn	upper front
J2		Conn, 2x22 card edge	Middle Detector Conn	upper front
J3		Conn, 2x22 card edge	Front Detector Conn	upper front
J4		Conn, 25 D F	Sample Intro. Dev. 1 Conn	top edge
J5		Conn, 25 D F	Sample Intro. Dev. 2 Conn	top edge
J6		Con, 15 D F	Analog Out and Integ Conn	top edge
J7		Con, 2x10 M	Temperature Input Conn	top edge
J8		Con, 34 hdr	Injector EFC Conn	upper front
J9		Con, 34 hdr	Detector EFC Conn	upper front
J10		Con, 40 hdr	Power PWA Conn	mid front
J11		Con, 4 M	Debug Conn	mid rear
J12		Con, 26 hdr	Printer Conn	mid edge
J14		Con, 96 DIN M	Com PWA Conn	lower rear
J15		Con, 96 DIN F	ROM PWA Conn	lower rear
J17		Con, 50 hdr	Front Panel Conn	lower front
J18		Con, 72 SIMM	DRAM Module Conn	lower rear
TP1	+5V	Test Point	+5V	upper rear
TP2	GND3	Test Point	Ground	upper front
TP3	+15V	Test Point	+15V	upper rear
TP4	-15V	Test Point	-15V	upper rear
TP5	-5V	Test Point	-5V	upper rear
TP6	+5.25V	Test Point	+5.25V	upper rear
TP8	+24V	Test Point	+24VPWR. Input for DC PS.	upper rear
TP9	-24VUNREG	Test Point	-24VUNREG	upper rear
S1	MODE "On"= closed "Off"=open	DIP Switch, 4-poles: S1-1,2,3,4.	Select softw. mode of operation: 1,2,3,4 (O=open, C=closed.) C,O,O,O=3800 product sw. O,O,O,C=ETS-FT or ETS-GC C,O,O,C=CBug in ETS-FT,ETS-GC	mid rear
S2	BREAK	Push-button Switch (May be removed from future production boards)	Causes a BREAK interrupt for softw. debugging. For softw. dev. only. May be removed from future production boards.	lower front
S3	RESET	Push-button Switch	Causes a CPU and system reset and reload of FPGA code.	lower front
CR2	DIAG1	LED, green	Diagnostics (future use)	mid rear
CR3	DIAG2	LED, green	Diagnostics (future use)	mid rear
CR4	DIAG3	LED, green	Diagnostics (future use)	mid rear
CR5	DIAG4	LED, green	Diagnostics (future use)	mid rear
CR6	HALT	LED, red	CPU in Halted state (fault)	lower front
CR7	RESET	LED, red	CPU in RESET state.	lower front
CR8	+5V	LED, green	+5V	lower front
CR9	STOP	LED, yellow	CPU in Stopped state. Running STOP instruction = idle. On and off during normal run.	lower front
CR10	LOAD	LED, green	FPGA config. code loaded OK.	mid rear

Note: The terms "front", "rear",. etc. refer to locations on board mounted in the GC.

Inputs to DC Power Supplies

Unregulated power is received on lines +24VPWR, +24VGEN and -24VUNREG of the Power PWA Connector J10.

+24VPWR: +24V unregulated. Input to the +5V logic supply and the +15V and +5.25V analog supplies. +24VPWR is also distributed to the EFC connectors J8 and J9.

+24VGEN: +24V unregulated. Feeds DC loads which are accessed by customers and which are considered more likely to experience short circuits: detectors, valves, motors, etc.

-24VUNREG: -24V unregulated. Input to the -15V and -5V analog supplies.

Each of these power input lines is independently fused on the Power PWA where it is generated.

DC Power Supply Outputs

+15V: +15VDC ±5% when +24VPWR > 19V.
Supplies analog circuitry including ADC and DAC and voltage references.

+5.25V: +5.25VDC ±5% when +24VPWR > 19V.
Supplies analog circuitry.

+5V: +5VDC ±3% when +24VPWR > 10V
Supplies the CPU, memory and logic.

-5V: -5VDC ±5% when +24VPWR > 19V.
Supplies analog circuitry.

-15V: -15VDC ±5% when +24VPWR > 19V.
Supplies analog circuitry including ADC and DAC and -5VDC regulator.

VBAT: +2.7 to +3.3VDC. Battery output.
Is used to generate SRAMVCC which powers Clock-calendar and Static RAM.

PFI: logic signal: Power Fail Interrupt. Is asserted when +24VPWR goes below +19V.